MP3423

9A, 600kHz High Efficiency, Synchronous Step-Up Converter with Output Disconnect in 2x2mm QFN Package

The Future of Analog IC Technology

DESCRIPTION

The MP3423 is a high-efficiency, synchronous, current-mode, step-up converter with output disconnect.

The MP3423 starts up from an input voltage as low as 1.9V, while providing inrush current limiting and output short-circuit protection. The integrated P-channel synchronous rectifier improves efficiency and eliminates the need for an external Schottky diode. This P-channel disconnects the output from the input during shutdown.

The 600kHz switching frequency allows small external components, while the internal compensation and soft-start minimize external component count. The MP3423 provides a compact solution for a 5V output, 3.1A load requirement, using a supply voltage down to 2.8V.

The MP3423 is available in 14-pin QFN 2mmx2mm package.

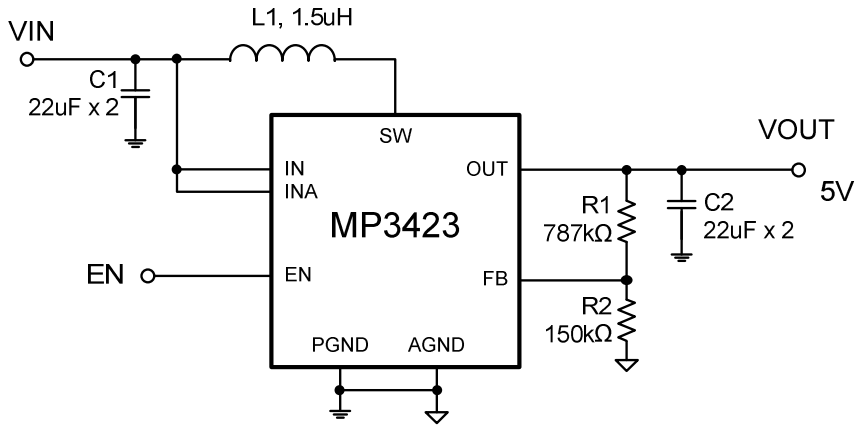
FEATURES

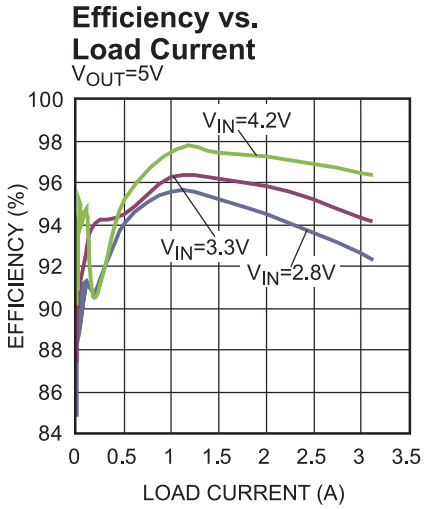
- Up to 98% Efficiency
- 1.9V to 5.5V Input Range
- 2.5V to 5.5V Output Range
- Internal Synchronous Rectifier
- 600kHz Fixed Switching Frequency
- 9A Typical Switch Current Limit
- 43uA Quiescent Current
- High Efficiency over Full Load Range
- Internal Soft-start and Compensation
- True Output Load Disconnect from Input
- OCP, SCP, OVP and OTP Protection
- Small 2x2mm QFN14 Package

APPLICATIONS

- Battery-Powered Products
- Power Banks, Juice Packs, Battery Back-up Units
- USB Power Supply
- Consumer Electronic Accessories
- Tablets

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3423GG	QFN-14 (2mmX2mm)	*See Blow*

* For Tape & Reel, add suffix –Z (e.g. MP3423GG–Z)

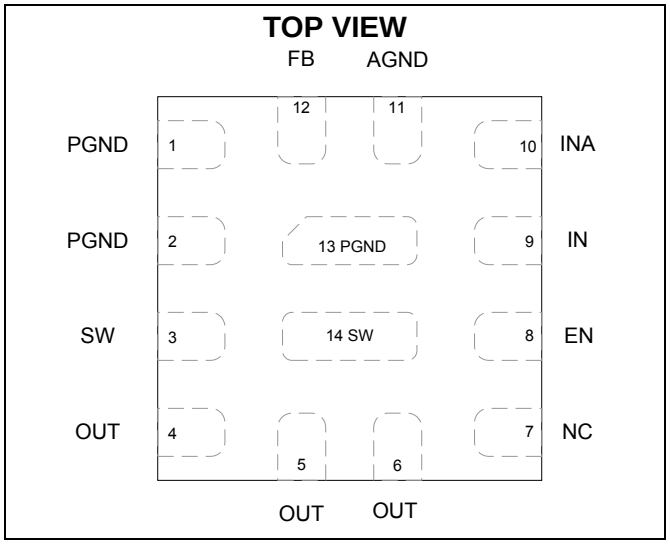
TOP MARKING

DAY

LLL

DA: product code of MP3423GG;
Y: year code;
LLL: lot number;

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

SW Pin .....-0.3V to +6.5V (10V for <5ns)
All other Pins ..... -0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
.....1.56W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....-65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 1.9V to 5.5V
V_{OUT} ..... 2.5V to 5.5V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-14 (2mmx2mm)	80	16	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, T_J= -40°C to125°C, typical values are tested at T_J =25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min.	Typ.	Max.	Units
Voltage Range						
Start Operating Input Voltage	V_{IN}		1.9		5.5	V
Quiescent Current	I_{Q_NS}	V_{EN}=V_{IN}=3.3V, V_{OUT}=5V, no load Measured on OUT pin, T_J=25°C		43	57	µA
		V_{EN}=V_{IN}=3.3V, V_{OUT}=5V, no load Measured on IN pin		0.3		µA
Shutdown Current	I_{SD}	V_{EN}=V_{OUT}=0V, Measured on IN pin, T_J=25°C		0.1	1	µA
IN UVLO Rising Threshold	$V_{UVLO\ IN-R}$	V_{IN} Rising T_J=25°C	1	1.3	1.6	V
IN UVLO Falling Threshold	$V_{UVLO\ IN-F}$	V_{IN} Falling, V_{OUT}=5V		650		mV
VOUT Start Switching Rising Threshold	V_{UVLO_OUT-R}	T_J=25°C		1.7	1.79	V
Step-up Converter						
Operation Frequency	F_{SW}	T_J=25°C	500	600	700	kHz
		-40°C≤T_J≤125°C	440	600	760	
Feedback Voltage	V_{FB}	T_J=25°C	795	807	819	mV
		-40°C≤T_J≤125°C	791	807	823	
Feedback Input Current	I_{FB}	V_{FB}=850mV		1	50	nA
NMOS On-Resistance	$R_{NDS\ ON}$			11		mΩ
NMOS Leakage Current	$I_{N\ LK}$	V_{SW}=5V		100		nA
PMOS On-Resistance	$R_{PDS\ ON}$			16		mΩ
PMOS Leakage Current	$I_{P\ LK}$	V_{SW}=5V, V_{OUT}=0V		0.1		µA
Maximum Duty Cycle	D_{MAX}		90	95		%
Linear Charge Current Limit(5)	I_{CH_LIMIT}	V_{OUT} =1.7V		0.7		A
		V_{OUT} =0V		0.2		A
NMOS Current Limit(5)	$I_{SW\ LIMIT1}$	V_{IN}=5V, V_{OUT}=3.3V		4		A
	$I_{SW\ LIMIT2}$	Duty=44%, Vin=2.8V, V_{OUT} =5V		9		A
Logic Interface						
EN High-Level Voltage	$V_{EN\ H}$		1.2			V
EN Low-Level Voltage	$V_{EN\ L}$				0.4	V
EN Input Current	I_{EN}	Connect to V_{IN}		10		nA
Protection						
Thermal Shutdown(5)				150		°C
Over Temperature Hysteresis(5)				20		°C

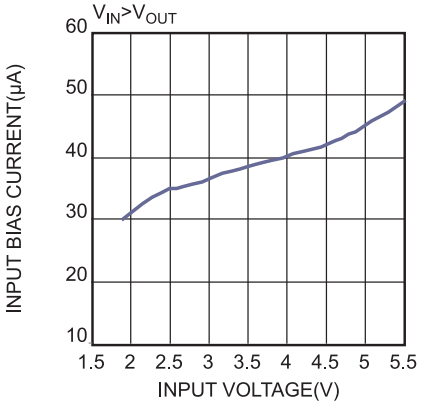
Notes:

5) Guaranteed by characterization, not production tested

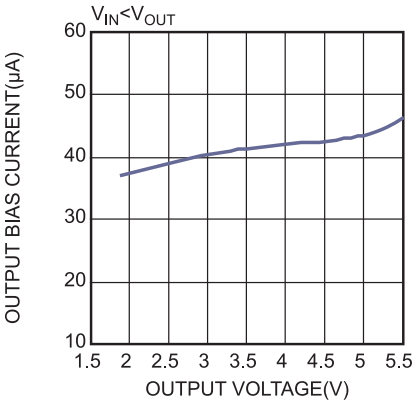
TYPICAL CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 5V, L=1.5uH, T_A = 25°C, unless otherwise noted.

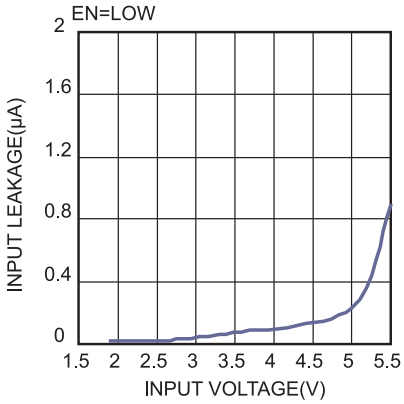
Quiescent Current vs. Input Voltage



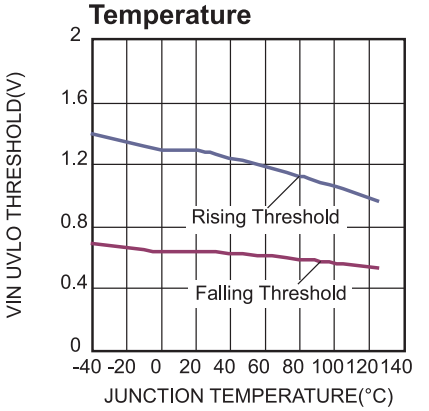
Quiescent Current vs. Output Voltage



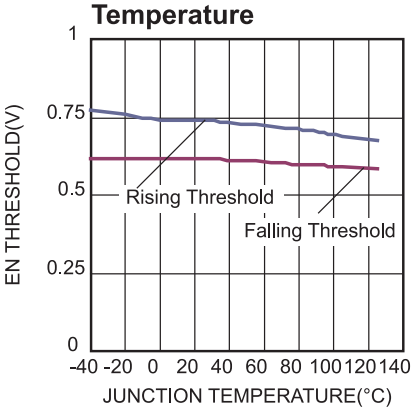
Shutdown Current vs. Input Voltage



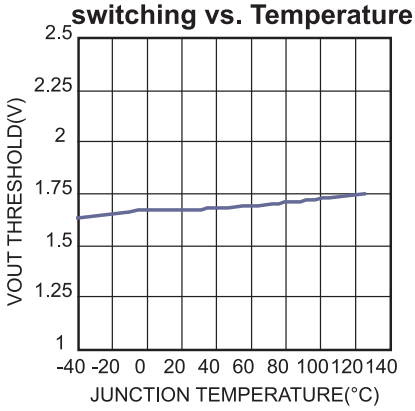
Input UVLO Threshold vs. Temperature



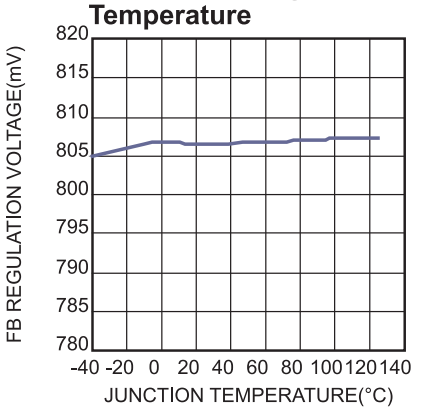
EN Threshold vs. Temperature



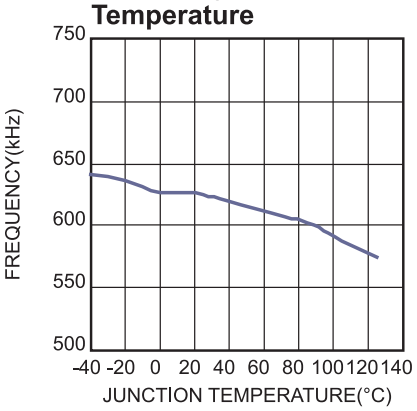
VOUT Rising Threshold for switching vs. Temperature



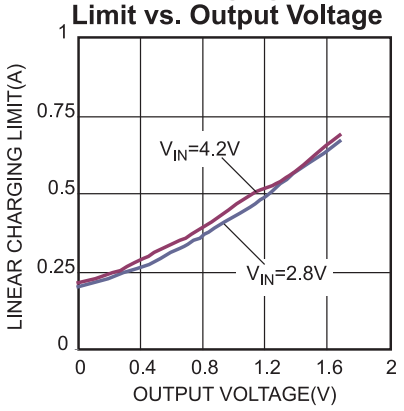
Feedback Voltage vs. Temperature



Frequency vs. Temperature



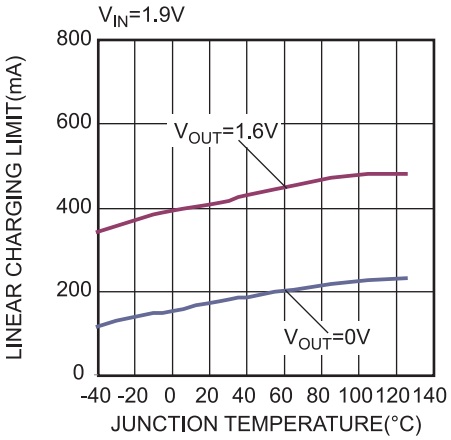
Linear-Charging Current Limit vs. Output Voltage



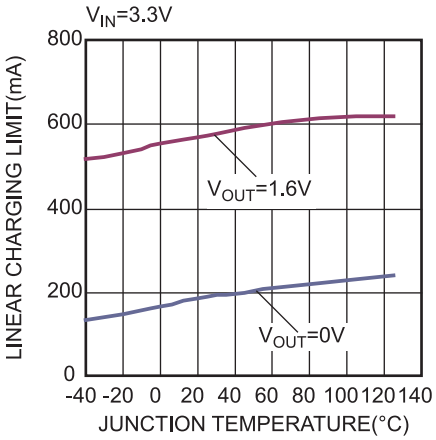
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L=1.5uH, T_A = 25°C, unless otherwise noted.

Linear-Charging Current Limit vs. Temperature



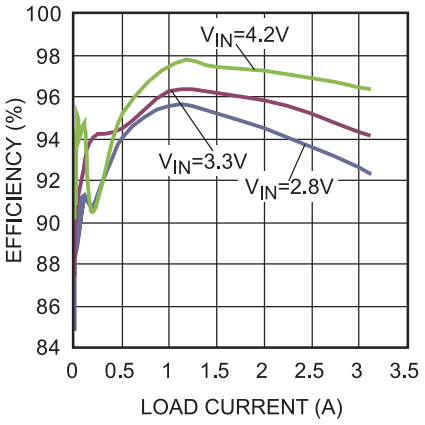
Linear-Charging Current Limit vs. Temperature



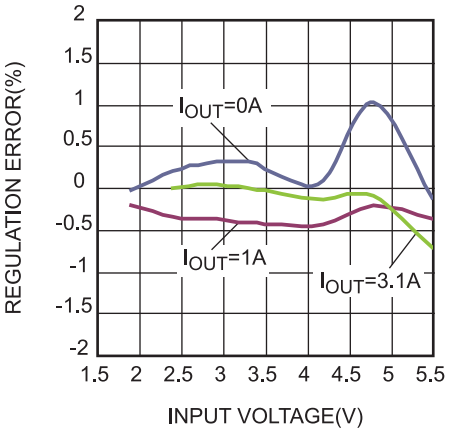
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L=1.5uH, T_A = 25°C, unless otherwise noted.

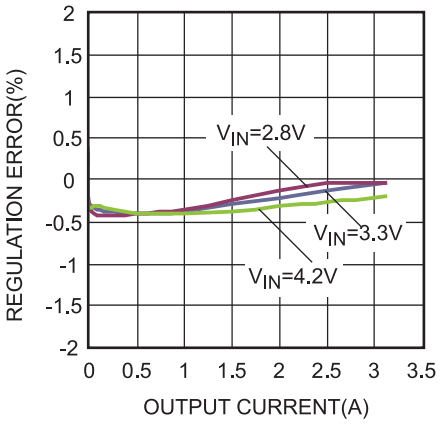
Efficiency vs. Load Current



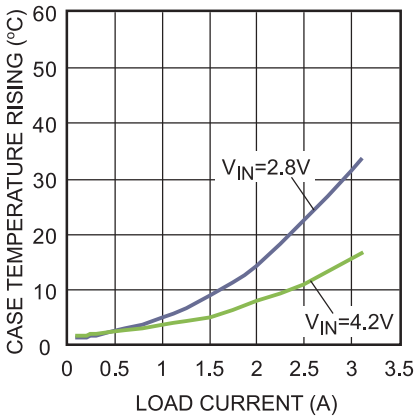
Line Regulation



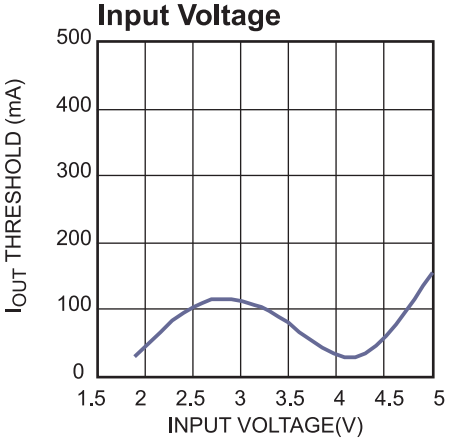
Load Regulation



Case Temperature Rising vs. Load Current



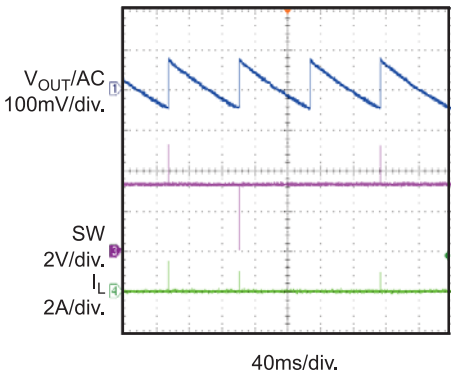
PSM Threshold vs. Input Voltage



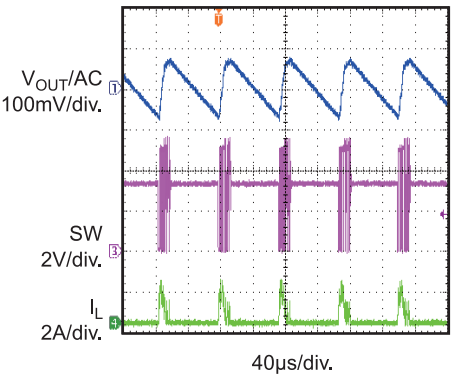
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L=1.5uH, T_A = 25°C, unless otherwise noted.

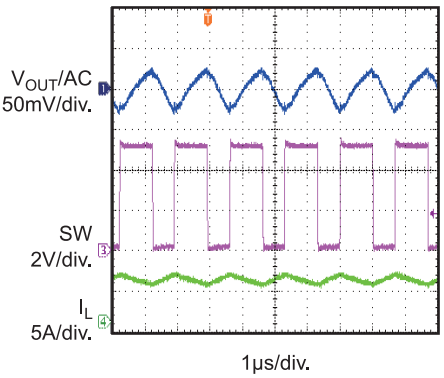
Output Voltage Ripple
Load = 0A



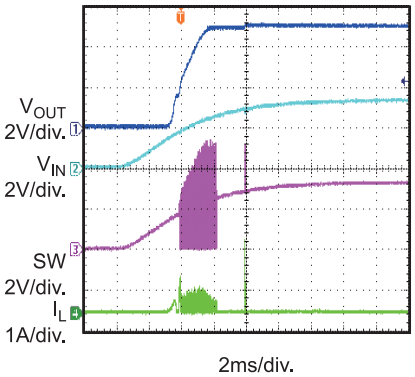
Output Voltage Ripple
Load = 0.1A



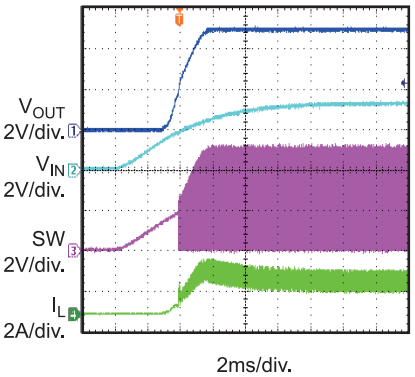
Output Voltage Ripple
Load=3.1A



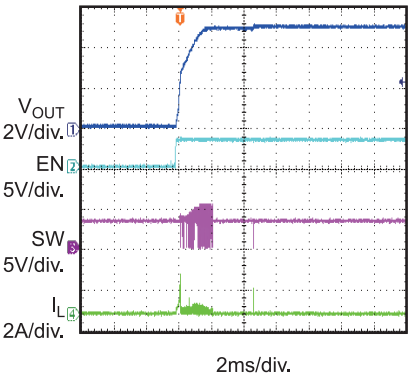
V_{IN} Startup
Load = 0A



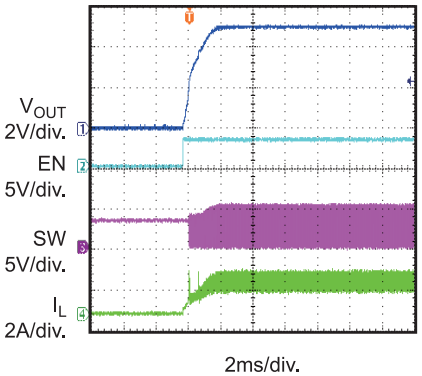
V_{IN} Startup
Load = 5Ω



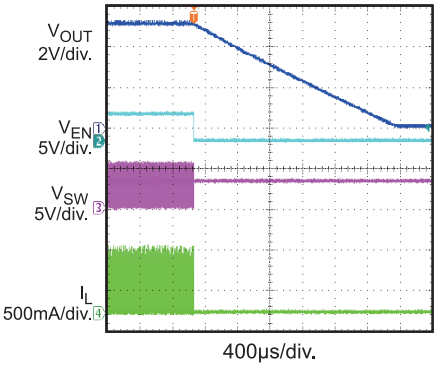
EN Start up
Load = 0A



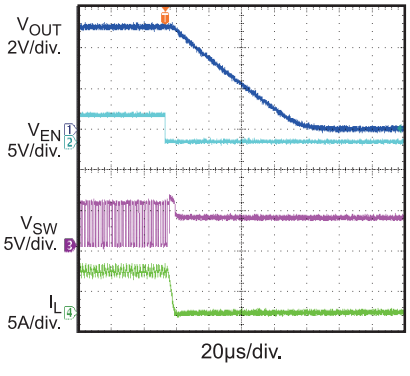
EN Startup
Load = 5Ω



EN Shutdown
Load=0.1A



EN Shutdown
Load=3.1A

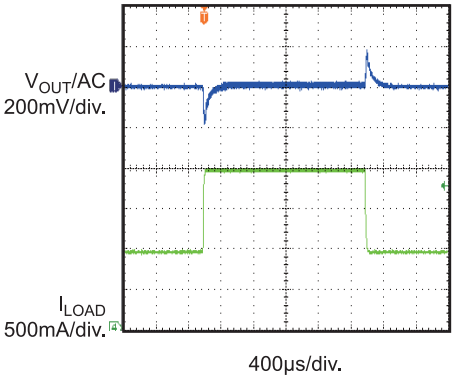


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L=1.5uH, T_A = 25°C, unless otherwise noted.

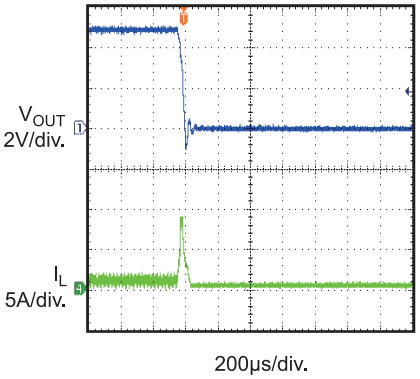
Load Transient

Load = 1A <--> 2A at 50mA/µs



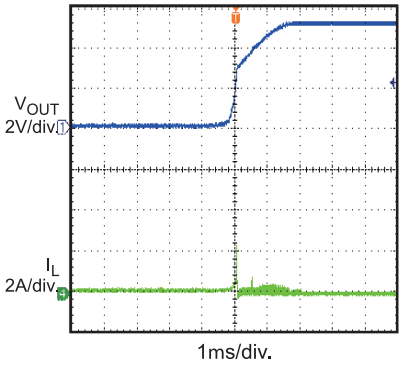
Short Circuit Entry

0.6A Load to Short



Short Circuit Recovery

Recover to 0A Load



PIN FUNCTIONS

Pin #	Name	Pin Function
1, 2, 13	PGND	Power Ground.
3, 14	SW	Power Switch Output. SW is the connection node of the internal NMOS switch and synchronous switch. Connect the power inductor between SW and input power. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage spikes.
4, 5, 6	OUT	Output Pin. OUT is the drain of the Internal Synchronous Rectifier MOSFET. Bias is derived from OUT when V_{OUT} is higher than V_{IN}. PCB trace length from OUT to the output filter capacitor(s) should be as short and wide as possible. OUT is completely disconnected from IN when EN is low due to the output disconnect feature.
7	NC	No Connect. Reserved for factory use only. Float or connect this pin to GND in the application.
8	EN	Chip Enable Control Input.
9	IN	Power Supply Input. The startup bias is derived from IN. Must be locally bypassed. Once OUT exceeds IN, bias comes from OUT. Thus, once started, operation is completely independent from IN.
10	INA	Power supply input for factory use only, must be connected to IN pin in the application.
11	AGND	Analog Signal Ground.
12	FB	Feedback Input to Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 2.5V to 5.5V

FUNCTION DIAGRAM

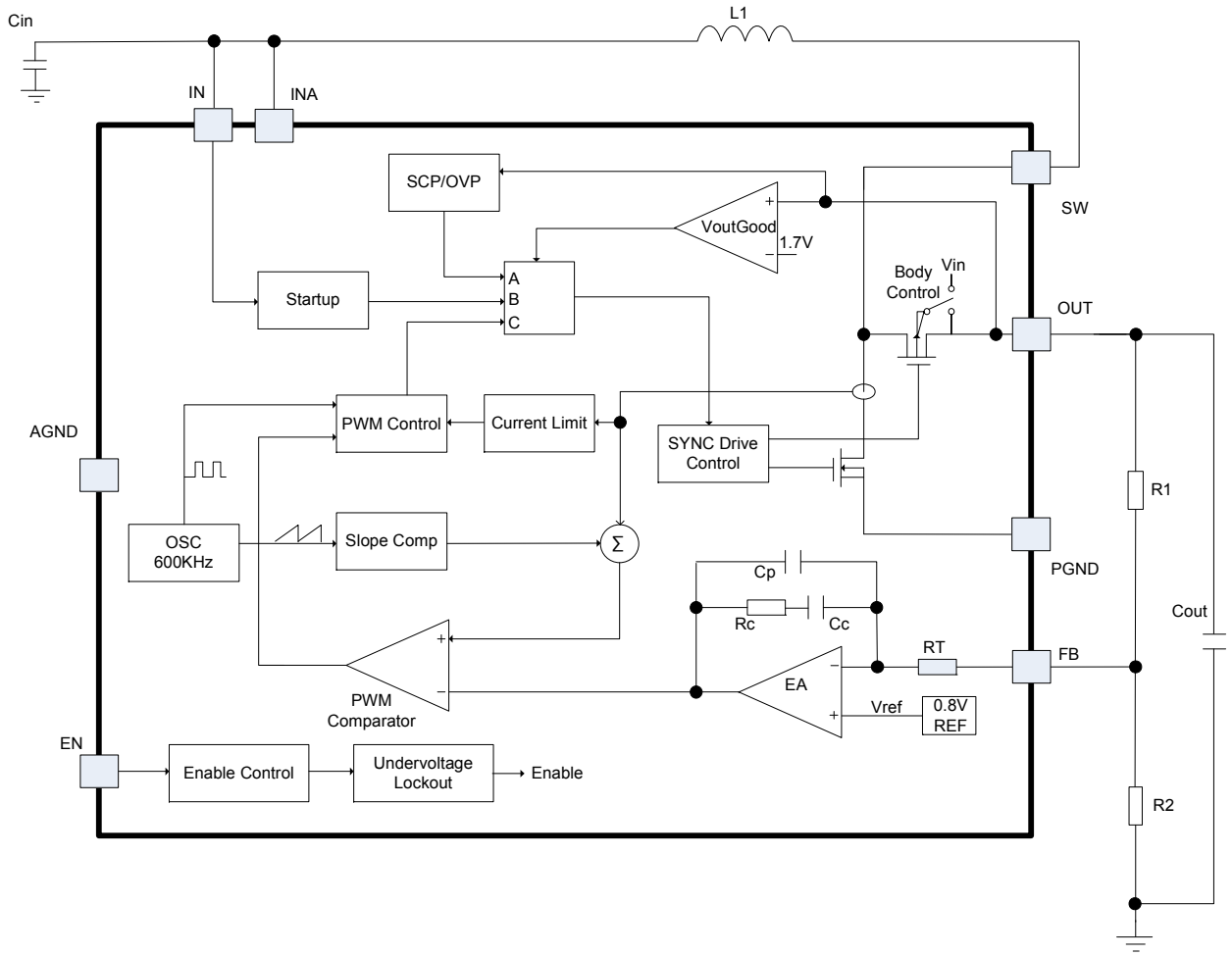


Figure 1: Functional Block Diagram

OPERATION

The MP3423 is a 600kHz, synchronous step-up converter with true output disconnect. It is packaged in a QFN 2X2-14 lead package. The device features fixed-frequency current mode PWM controls for excellent line and load regulation. Internal soft-start and loop compensation simplifies the design process and minimizes external components. The internal low RDSon MOSFETs, combined with frequency stretching operation, enables the device to maintain high efficiency over a wide load current range.

Start-Up

When the IC is enabled and the voltage on the IN pin exceeds V_{uvlo_in-R}, the MP3423 starts up in the linear charge period. During this linear charge period, the PMOS rectifier turns on until the output capacitor is charged to 1.7V. The PMOS current is limited to 0.2A when Vout is 0V to avoid inrush current. While the output ramps up, the PMOS current limit also increases and ramps to 0.7A at 1.7V output. This circuit also helps to limit the output current under short circuit conditions. Once the output is charged to 1.7V, the linear charge period elapses and the MP3423 starts switching in normal closed loop operation. In normal operation, with Vo lower than Vin+0.3V the MP3423 operates in step down mode with 4A typical peak current limit, and works in boost mode when Vo is higher than Vin+0.3V with 9A typical peak current limit.

Table 1: Work Mode during Startup

V_{OUT}<1.7V	Linear Charge Mode
$V_{OUT} \geqslant$1.7V & $V_{OUT} < V_{IN}$ + 0.3V	Down Mode
$V_{OUT} \geqslant$1.7V & $V_{OUT} \geqslant V_{IN}$ + 0.3V	Boost Mode

In down mode, gate of HS-FET is pulled to VIN, and it works with high impedance when HS-FET is on, the power-loss is high and regulation is bad in down mode. Down mode is designed for work in startup and SCP condition, it is not suggested to set MP3423 in down mode in normal work, unless the thermal and regulation will not affect the system performance.

Once the output voltage exceeds the input voltage, the MP3423 powers its internal circuits from Vout instead of Vin.

Soft-Start

The MP3423 provides soft-start by charging an internal capacitor with a current source. This soft start voltage continues to rise, following the FB voltage, during the linear charge period. Once the linear charge period elapses, and the voltage on this capacitor is charged, the reference voltage is slowly ramped up. The reference soft start time is typically 2ms from 0V to 0.807V.

The soft start capacitor is discharged completely in the event of a commanded shutdown, thermal shutdown or short circuit at the output.

Device Enable

Operation is enabled when the EN pin is switched high and placed into shutdown mode when low. In shutdown mode, the regulator stops switching and all internal control circuitry is off. The load is isolated from the input.

Power-Save Mode

The MP3423 will automatically enter power save mode (PSM) when the load decreases and resume PWM mode when the load increases. When the device goes into PSM, it lowers the switching frequency saving switching and driver losses, and switches to pulse skip mode if the load continues to decrease.

Error Amplifier

The error amplifier (EA) is an internally-compensated amplifier. The EA compares the internal 0.807V reference voltage against V_{FB} to generate an error signal. The output voltage of the MP3423 is adjusted by an external resistor divider. A voltage divider from V_{OUT} to ground programs the output voltage via the FB pin from 2.5V to 5.5V using the equation:

$$V_{OUT}=0.807V \times (1+R1/R2)$$

Set the value of R1 and R2 to achieve low quiescent current. R1 values larger than 600k are recommended for good stability and transient balance.

Current Sensing

Lossless current sensing converts the NMOS switch current signal to a voltage which is summed with the internal slope compensation. The summed signal is compared to the error amplifier output to provide a peak current control command for the PWM. Typical peak switch current limit is 9A. The switch current signal is blanked for about 60ns internally to enhance noise rejection.

Output Disconnect

The MP3423 is designed to allow true output disconnect by eliminating body diode conduction of the internal PMOS rectifier. This allows V_{OUT} to go to zero volts during shutdown, or isolate and maintain an external bias on V_{OUT}. It also allows for inrush current limit at start-up, minimizing surge current seen by the input supply. To obtain the advantage of output disconnect, there must not be an external Schottky diode connected between the switch pin and V_{OUT}.

Over Load and Short Circuit Protection

When an overload or a short circuit occurs, the output voltage will drop. If Vout drops below Vin+0.3V, the MP3423 will convert to step down mode. If Vout drops below 1.7V, the device will convert to linear charge mode. If Vout drops below about 70% of the nominal output voltage, the MP3423 will immediately shut down and re-start after about 40μs as a new power-on cycle.

Over Voltage Protection

If Vout is higher than 7V, boost switching stops. This prevents overvoltage from damaging the internal power MOSFET. When the output drops below 7V, the device resumes switching automatically.

Thermal Shutdown

The device contains an internal temperature monitor. The switches turn off if the die temperature exceeds 150°C. The device will resume normal operation below 130°C.

APPLICATION INFORMATION

COMPONENT SELECTION

Input Capacitor Selection

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. Ceramic capacitors are a good choice for input decoupling and should be located as close as possible to the device. A ceramic capacitor larger than 22μF is recommended to restrain V_{IN} ripple.

Output Capacitor Selection

The output capacitor requires a minimum capacitance value of 22μF at the programmed output voltage to ensure stability over the full operating range. A higher capacitance value may be required to lower the output ripple and transient ripple. Low ESR capacitors such as X5R or X7R type ceramic capacitors are recommended. Supposing that ESR is zero, the minimum output capacitor to support the ripple in the PWM mode could be calculated by:

$$C_O \geq \frac{I_O \times (V_{OUT(MAX)} - V_{IN(MIN)})}{f_S \times V_{OUT(MAX)} \times \Delta V}$$

Where,
$V_{OUT(MAX)}$ = Maximum output voltage
$V_{IN(MIN)}$ = Minimum Input voltage
I_O=Output current
f_S = Switching frequency
ΔV= Acceptable output ripple

A 1μF ceramic capacitor is recommended between the Out and PGnd pins. This reduces spikes on the SW node and improves EMI performance.

Inductor Selection

The MP3423 can utilize small surface mount chip inductors due to its 600kHz switching frequency. Inductor values between 1μH and 2.2μH are suitable for most applications. Larger values of inductance will allow slightly greater output current capability by reducing the inductor ripple current, but larger value inductance increases component size. The minimum inductance value is given by:

$$L \geq \frac{V_{IN(MIN)} \times (V_{OUT(MAX)} - V_{IN(MIN)})}{V_{OUT(MAX)} \times \Delta I_L \times f_S} \quad (3)$$

ΔI_L=Acceptable inductor current ripple

The inductor current ripple is typically set for 30% to 40% of the maximum inductor current. The inductor should have low DCR (series resistance of the inductor current without saturating windings) to reduce the resistive power loss. The saturated current (I_{SAT}) should be large enough to support the peak current.

PCB Layout Considerations

PCB layout for high frequency switching power supplies can be critical. Poor layout can result in reduced performance, excessive EMI, resistive loss and system instability.

The steps below ensure good layout design.

1. The output capacitor must be placed as close as possible to the OUT pin, with minimal distance to PGND. A small decoupling capacitor should be paralleled with the bulk output capacitor and placed as close as possible to the OUT Pin. This is very important to reduce the spikes on the SW Pin and improve EMI performance.
2. The input capacitor and inductor should as close as possible to the IN and SW pins. The trace between the inductor and the SW pin should be wide and as short as possible.
3. The feedback loop should be far away from all noise sources such as the SW pin. The feedback divider resistors should be as close as possible to the FB and AGND pins.
4. The ground return of the input/output capacitors should be tied as close as possible to the PGND pin with a large copper GND area. Vias around the GND pin are recommended to lower the die temperature.
5. INA pin must be connected to IN. NC pin can either float or be connected to GND.

Figure 2 recommends components placement for MP3423.

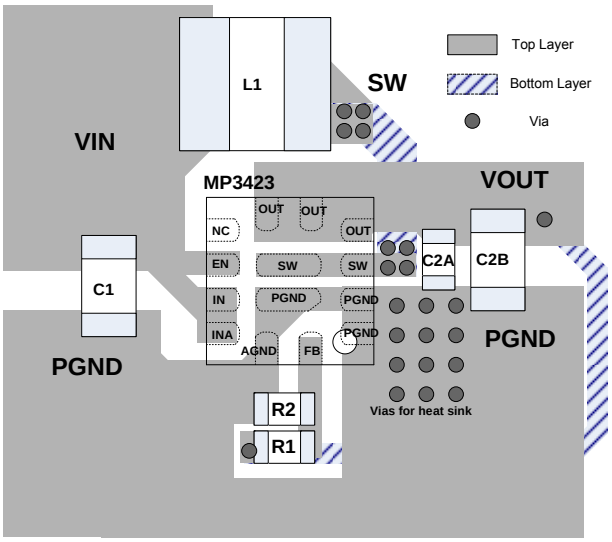


Figure 2: Layout Recommendation

Design Example

Below is a design example following the application guidelines for the following specifications:

Table 2, Design Example

V_{IN}	2.8V-4.2V
V_{OUT}	5V
I_{OUT}	0A-3.1A

The typical application circuit for V_{OUT} = 5V in Figure 3 shows the detailed application schematic, and is the basis for the typical performance waveforms. For more detailed device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

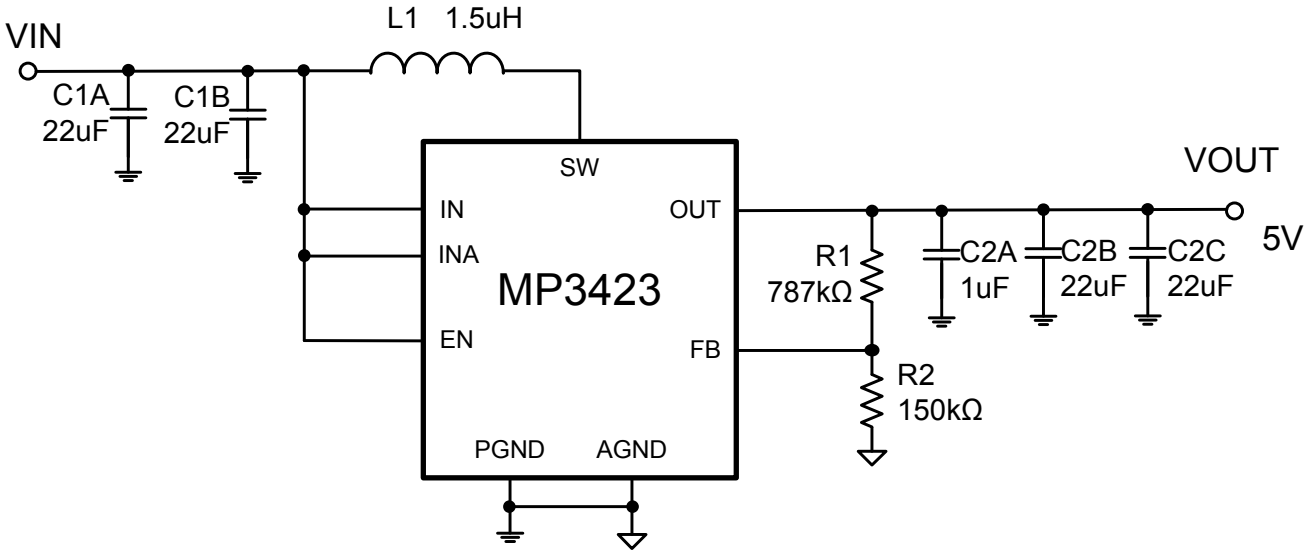
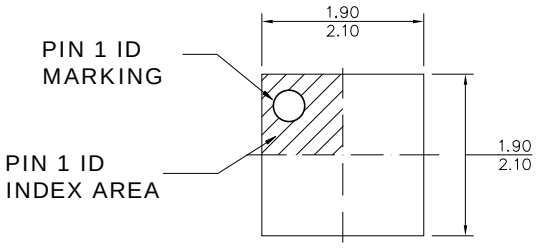


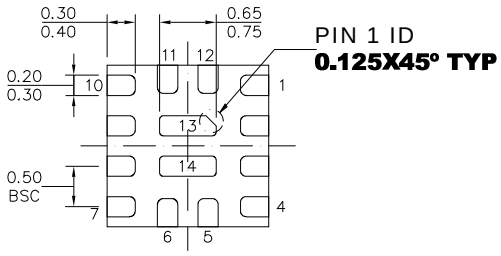
Figure 3: Typical Boost Application Circuit, V_{IN}=2.8V to 4.2V, V_{OUT}=5V, I_{OUT}=0A-3.1A

PACKAGE INFORMATION

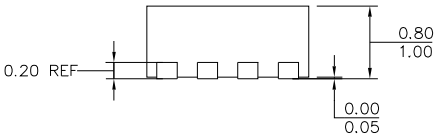
QFN14 (2mmX2mm)



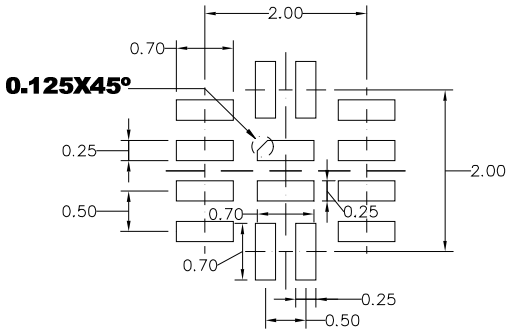
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.